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Patent Claims

1. A patterning method,
 - 5 in which the following method steps are performed:
application of an auxiliary layer (14, 14c) to a carrier material (12, 10c),
application of a mask layer (16, 16c) to the auxiliary layer (14, 14c) prior to the production of a cutout
10 (18, 18c),
patterning of the mask layer (16, 16c) by means of a lithographic method
patterning of the auxiliary layer (14, 14c) and of the carrier material (12, 10c) with production of a cutout
15 (18, 18c) in accordance with the patterned mask layer (16, 16c),
afterward expansion of the cutout (18, 18c) in the region of the auxiliary layer (14, 14c) by isotropic etching-back, the cutout (18, 18c) in the region of the carrier material (12, 10c) not being expanded or not
20 being expanded to as great an extent as in the region of the auxiliary layer (14, 14c),
filling of the expanded cutout (18b, 18d) with a filling material (22, 22c),
25 removal of the auxiliary layer (14, 14c) after filling,
patterning of the carrier material (12, 10c) using the filling material (22, 22c) as a mask and with production of at least one further cutout.
- 30 2. The method as claimed in claim 1, characterized by the following step:
planarization of the filling material (22, 22c) prior to the repeated patterning.
- 35 3. The method as claimed in one of the preceding claims, characterized in that it is used for producing

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a minimum feature size of less than one hundred nanometers.

4. The method as claimed in claim 3, characterized in
5 that it is used for producing a minimum feature size of less than fifty nanometers.

5. The method as claimed in one of the preceding claims, characterized by the following steps:
10 formation of a mask layer (12) as carrier material prior to the application of the auxiliary layer (14), patterning of a basic material (10) using the mask layer (12) after the patterning of the carrier material (12) using the filling material (22).

15 6. The method as claimed in one of the preceding claims, characterized by the following step:
use of a semiconductor material (10c) as carrier material (10c), in particular a monocrystalline
20 semiconductor material (10c).

7. The method as claimed in claim 6, characterized by the following step:
formation of at least one layer (50, 52) in the
25 expanded cutout (18d) prior to filling, in particular of an electrically insulating layer (50) and of an electrically conductive layer (52).

8. The method as claimed in claim 7, characterized in
30 that the layer (50, 52) is patterned by a method as claimed in one of claims 1 to 5.

9. The method as claimed in one of claims 6 to 8, characterized by the following steps:
35 filling of the further cutout with a further filling material (70),

removal of the filling material (22, 22c) serving for patterning after the filling of the further cutout.

10. The method as claimed in one of claims 6 to 8,
5 characterized by the following steps:
partial removal of the filling material (22, 22c) from the cutout (18, 18c), one part of the bottom of the cutout (18, 18c) being uncovered and another part of the bottom of the cutout (18, 18c) remaining covered
10 with filling material (22, 22c).

11. The method as claimed in one of claims 6 to 10, characterized by the following step:
oxidation of the semiconductor material (10c) in the
15 region between the cutout (18c) and the further cutout, in particular in an intermediate region extending from the cutout (18c) to the further cutout,
preferably prior to the removal of the filling material (22c) and preferably after the production of an
20 oxidation protective layer (80) on at least one sidewall of the further cutout.

12. A field effect transistor (100),
having two channel connection regions (104, 106),
25 having a control region (52, 62) containing at least two control region sections,
having an active region that is formed as a projection (56) of a monocrystalline substrate (10c) and is arranged between the channel connection regions (104, 106) on the one hand, and between two control region
30 sections, on the other hand,
and having insulating regions (50, 60) that are electrically insulating and are arranged between the control region sections and the active region (56),

the projection (56) being isolated from the substrate (10c) at its base by an insulating material (82) that is electrically insulating,
and the insulating material (82) ending laterally at
5 the projection (56) in the monocrystalline substrate (10c).

13. The field effect transistor (100) as claimed in claim 12, characterized in that two side areas of the
10 projection (56) that lie at the base of the projection transversely adjoin two substrate areas of the substrate (10c) that are arranged in two planes spaced apart from one another, the distance (D) being greater
15 than one nanometer, greater than three nanometers or greater than five nanometers.

14. The field effect transistor (100) as claimed in claim 12 or 13, characterized in that the control
20 region sections are formed on the two side areas of the projection (56).

15. The field effect transistor (100) as claimed in one of claims 12 to 14, characterized in that the
25 insulating material (82) does not project beyond at least one side area of the projection (56).